Single Network Structure for Stuck-at and Bridging Fault Analysis and Diagnosis of Exclusive-OR Sum of Products Reed-Muller Canonical Circuits

Geetha V., Devarajan N. and Neelakantan P. N.

Abstract— In this paper, a testable design with good fault identification capability is used for analysis and diagnosis of AND-bridging and double stuck-at faults in Exclusive-OR Sum of Product Reed-Muller canonical circuits, independent of the function for a given number of inputs. Factors of identifiability and distinguishability have been defined and determined. Further, a compact method of representing the circuit outputs has been adopted for ease of tabulation and comparison. Simulations of AND-bridging and Double stuck-at faults for a few random functions have been carried out through MATLAB coding. From the test results, it was found that the fault detection for the set of random functions was more than 90% for most of the functions except few cases, with just n+5 test vectors compared to 2^n test vectors required for conventional testing. The location of the fault can also be diagnosed through the output sets.

Index Terms— Reed-Muller Canonical Form, Exclusive-OR Sum of Products, Testable Realization, AND-bridging fault ,Double stuck-at fault

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1 INTRODUCTION

THE faults in digital circuits can be classified broadly as single stuck-at-faults, multiple stuck-at-faults, stuck-open faults, stuck-on faults, bridging faults, path delay faults, transient faults etc. Any arbitrary logic function, in general, can be expressed in Reed-Muller Canonical (RMC) form as F = (a0 ⊕ a1x1* ⊕ a2 x2* ⊕…⊕ anxn* ⊕ an+1 x1* x2* ⊕ …⊕ am x1* x2*…xn*)where, x_n* can be x_n or its complement, a_n is either 0 or 1 and m = 2^n-1. However, there can be variations in such forms. The different types are Fixed Polarity RMC (FPRM), Positive Polarity RMC (PPRM), Generalized RMC (GRM) and Exclusive-OR Sum-of-Products RMC (ESOP RM). The FPRM has a restriction that the variables in any of the product terms have to be of the same type namely complementary or non-complementary. For PPRM, the complementary form of variables is not allowed. The GRM may contain both complementary and non-complementary types but the combination of the variables should be unique. The ESOP form does not have any such restriction. Also the ESOP form has the least number of product terms and hence needs the least number of AND gates and is very much suitable for hardware implementation.

Extensive research has been carried out in the field of testing of digital circuits to reduce the number of input vectors. The cardinality of the test vectors proposed by many authors becomes prohibitively excessive for large number of input variables. It was demonstrated that Single stuck-at fault detection can be achieved with only n+5 test vectors [6]. The same structure was extended for OR-bridging fault analysis and is explained in [15] and [16]. In this paper, it is shown through Matlab simulations that AND-bridging and Double stuck-at fault detection and diagnosis could also be achieved with the same n+5 test vectors considering all input lines, control lines and intermediate gate outputs.

Two quantitative indices, called identifiability factor and distinguishability factor are considered for comparison of the testability nature of given circuits. The identifiability factor is defined as the ratio of the number of faults correctly identified by the test set to the total number of possible faults of the type considered. The existence of faults can be recognized from the set of outputs measured which will be different from the fault-free circuit. The distinguishability factor pertains to the identical set of outputs among different faults, but the output set of each being very much different from the non-faulty case. The existence of even a small percentage of distinguishability may not mean the circuit is not reliable, since it is still possible to identify the faulty condition of the circuit and take appropriate remedial action. The set of binary values for an output is converted into its decimal equivalent for convenience in comparison and ease of tabulation.

2 LITERATURE SURVEY

A PPRM network for detection of stuck-at faults with a universal test set of size n+4, n being the number of data inputs, was proposed in [1]. Though quite good for self-testing, the method is economical only for the specified form, which obviously has more number of product terms than the other forms in most cases. Multiple stuck-at fault detection for ESOP circuits was carried out in [2]. However, since the cardinality is 2n+6+ $\sum nC_e$, e = 0 to j, the order of ESOP expression, the test set is not universal and also is too large to be practical for large input functions. Stuck-at and bridging faults with a universal test set for PPRM network has been reported in [3]. Multiple fault detecting GRM realizations was proposed in [4].

Reference [5] described an ESOP implementation with a universal test set of size n+6 for single stuck-at faults only. In [6] it was demonstrated that single stuck-at fault detection can be achieved with only n+5 test vectors. It was shown in [7] that 2n+s+3 test vectors are required for single stuck-at fault detections in GRM / ESOP circuits while 2n+s vectors are required for detection of AND/OR-bridging faults in such circuits , where s is the number of product terms in the logic function. Here too, the test set is not universal as it depends on s, the number of product terms of the function. References [8], [9] proved that a test sequence of length 2n+8 vectors is sufficient to detect all single stuck-at and bridging faults. Two new methods, each with a small modification in this scheme with ESOP RMC circuits had been proposed for analysis and diagnosis of single stuck-at faults [10], [11].

In [12],[13],[14], it was demonstrated how the RMC forms help in the detection of various digital faults and how to determine the best polarity among them. It was proved that test vectors for multiple fault detection and diagnosis in digital circuits could be generated using Neural Network with different training algorithms [15]. Reference [16] proposed a new test pattern generation algorithm using Neural Network which requires additional gates. The analysis and diagnosis of OR-bridging faults in any of the pairs of data and control lines and OR-bridging faults including intermediate gate outputs of the ESOP RMC circuits was proposed in [17], [18]. This paper is an extension of [18] which also analyses the AND-bridging and double stuck-at faults of the ESOP RMC circuits with minimal test vectors.

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3 MATERIALS AND METHODS

3.1 Network Structure

The network structure of the scheme is the same as that proposed in [6] and is shown in Fig. 1. It comprises a literal complementing XOR block, an AND block, an XOR function tree block, which implements the required logic function as also two additional outputs O_1 and O_2 obtained through a separate AND gate and an OR gate. The actual data inputs to the system are x_1, x_2 …. x_n. Additionally, the scheme requires four control inputs c_1 to c_4. The literal-complementing block produces the complements of the literals used in the function. Only those literals appearing in complemented form require an XOR gate in this block.

The literals of each product term P_1, P_2, ..P_m are combined through an AND gate and hence the number of AND gates required is the same as the number of product terms in the logic function. Further, each of the AND gates of this block has an additional input from one of the control lines depending on the number of gates used in the XOR tree block producing the final function F. Finally, all the data and complementary gate outputs are applied to a separate AND gate and an OR gate, producing auxiliary outputs O_1 and O_2, to aid in the detection of faults which cannot be differentiated by the main function output F alone.

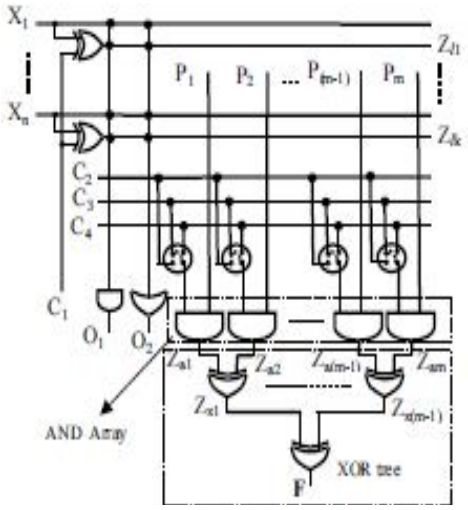

Fig.1 Generalised Network structure

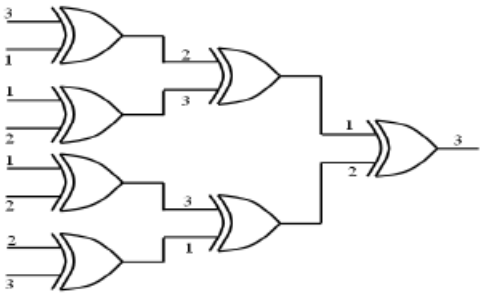

Fig.2 Control Input Determination

The required control lines are determined as illustrated above (Fig. 2). Draw the XOR gate tree for the required product terms of the given function. Assign the numerals 1, 2 and 3 respectively to the two inputs and the output of the final XOR gate producing the function output F. Consider each XOR gate connected to the inputs of the final XOR gate considered. Assign the outputs of these XOR gates with the same numbers as the inputs of the final XOR gate. If the output of the XOR gate considered is 1, then assign 2 and 3 to its inputs; else if the output is numbered 2, assign 3 and 1 to its input. Now consider the next earlier input stage and assign the numerals in the similar manner according to the output points connected.

3.2 Test Vectors

The test set has (n+5) vectors; each of the vectors is (n+4) long, 'n' being the number of data inputs. The first four columns of the matrix represent the control inputs c_1 to c_4 while the remaining n columns that of the data inputs are x_1 to x_n. The generalized test set is shown in Table 1.

TABLE 1
GENERALIZED TEST SET

c_1	c_2	c_3	c_4	x_1	x_2	...	x_n
0	0	0	0	0	0	...	0
0	0	1	1	1	1	...	1
0	1	0	1	1	1	...	1
0	1	1	1	1	1	...	1
0	1	1	1	0	1	...	1
0	1	1	1	1	0	...	1
0	1	1	1	1	1	...	1
.	.	.	.	.	.		
.	.	.	.	.	.		
.	.	.	.	.	.		
0	1	1	1	1	1	...	0
1	0	0	0	0	0	...	0

3.3 Algorithm

1. Set up the circuit as in Fig. 1.
2. Determine and connect the control lines c_1 to c_4 as explained.
3. Apply the test vectors as given in Table 1, one by one.
4. For each test vector, determine the fault free outputs F, O_1 and O_2.
5. Obtain the decimal equivalents of each of the above binary output sets.
6. Simulate the AND-bridging and double-stuck-at faults with various possible combinations of the control inputs, data inputs and intermediate gate outputs and get the corresponding decimal outputs.
7. Compare the set of outputs with the predetermined fault-free outputs.
8. If the two output sets match exactly, it implies that a fault, if present, is not identifiable or detectable; else, the fault is a detectable one.
9. Repeat steps 4 to 8 for all the ten functions and for the specified faults.
10. Calculate the identifiability factor and distinguishability factor for each type of fault.

4 RESULTS AND DISCUSSION

The following ten random functions were considered and AND-bridging and double stuck-at faults are simulated using MATLAB coding and the consolidated results are tabulated in Tables 4 and 9.

$F_1 = x_1 \oplus x_2x_3 \oplus x_1'x_2x_3$

$F_2 = x_1x_2 \oplus x_2'x_3 \oplus x_3'x_4 \oplus x_1x_2x_3$

$F_3 = x_1' \oplus x_2x_3'x_4 \oplus x_3x_4' \oplus x_2'x_3 \oplus x_1x_4x_5$

$F_4 = x_1x_2' \oplus x_2x_3x_4' \oplus x_4x_5'x_6 \oplus x_2x_5 \oplus x_2'x_5' \oplus x_3'x_2x_1 \oplus x_4x_6$

$F_5 = x_1'x_2x_3 \oplus x_4x_5x_6 \oplus x_4'x_6'x_7 \oplus x_3x_5x_7$

$F_6 = x_1x_2'x_3 \oplus x_4'x_5x_6' \oplus x_7x_8' \oplus ' \oplus x_1'x_6 \oplus x_3'x_4 \oplus x_1x_5 \oplus x_4x_5' \oplus x_5x_7 \oplus x_8x_3x_1 \oplus x_3x_5'x_8$

$F_7 = x_1x_2'x_3' \oplus x_4x_5'x_6 \oplus x_7'x_8x_9 \oplus x_1'x_4'x_9' \oplus x_2x_5' \oplus x_3x_5$

$F_8 = x_1'x_2x_3' \oplus x_4'x_5'x_6 \oplus x_7x_8'x_9' \oplus x_{10} \oplus x_6'x_7 \oplus x_8x_{10}$

$F_9 = x_1 \oplus x_2'x_3x_4' \oplus x_5'x_6x_7' \oplus x_8x_9x_{10} \oplus x_{10}'x_{11} \oplus x_1x_3x_9$

$F_{10} = x_1'x_2 \oplus x_3x_4'x_5 \oplus x_6x_7'x_8x_9 \oplus x_{10}x_{11}'x_{12} \oplus x_1x_2x_3' \oplus x_4'x_7$

As an illustration, the three variable function $F_1 = x_1 \oplus x_2x_3 \oplus x_1'x_2x_3$ is considered. The network structure and the set of test vectors for the function F_1 is shown in Fig. 3 and Table 2 respectively.

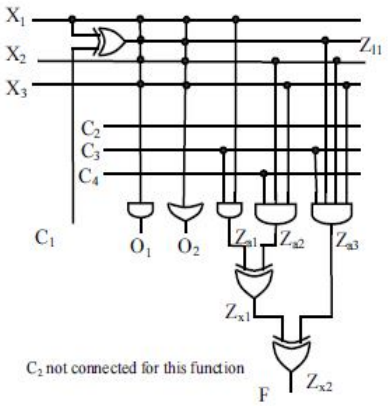

Fig. 3 Circuit for $F = x_1 \oplus x_2x_3 \oplus x_1'x_2x_3$

TABLE 2
TEST VECTORS FOR $F = x_1 \oplus x_2x_3 \oplus x_1'x_2x_3$

c_1	c_2	c_3	c_4	x_1	x_2	x_3
0	0	0	0	0	0	0
0	0	1	1	1	1	1
0	1	0	1	1	1	1
0	1	1	1	1	1	1
0	1	1	1	0	1	1
0	1	1	1	1	0	1
0	1	1	1	1	1	0
1	0	0	0	0	0	0

4.1 AND-Bridging Faults

The bridging faults are considered as a special case of multiple faults. A detailed numerical illustration for three variable AND-bridging faults is given below.

Function considered: $F_1 = x1 \oplus x_2x_3 \oplus x_1'x_2x_3$

Fault-free output set {F, O_1, O_2} = {126, 112, 127}

The outputs of AND-bridging faults at lines c_1 in combination with c_2, c_3, c_4, x_1, x_2 , x_3, zl_1, za_1, za_2, za_3, zx_1 and zx_2 are tabulated in Table 3(a) and 3(b).

TABLE 3(a)

AND-BRIDGING FAULTS INVOLVING c1 FOR FUNCTION F1

	c_1c_2	c_1c_3	c_1c_4	c_1x_1	c_1x_2	c_1x_3
F	126	120	6	120	86	86
O_1	112	112	112	0	0	0
O_2	126	126	126	126	126	126

TABLE 3(b)

	c_1zl_1	c_1za_1	c_1za_2	c_1za_3	c_1zx_1	c_1zx_2
F	46	40	6	46	80	0
O_1	0	112	112	112	112	112
O_2	127	126	126	126	126	126

Total No. of fault location pair combinations

$= (nc+ nx+nzl+nza+nzx)\ C_2 = 13C_2 = 78$

Total number of possible bridging faults for the given three variable function used is 78.

From the simulation results it was found that the number of unidentifiable faults as 11.

∴The Identifiability Factor is

(78 - 11) / 78*100 = 85.90%.

For the given example, the output sets that get repeated are as follows:

{6, 112, 126} 2 times
{62, 112, 127} 5 times
{80, 112, 127} 2 times
{80, 112, 127} 2 times
{86, 0, 126} 2 times
{86, 80, 127} 2 times
{86, 112, 127} 5 times
{94, 112, 127} 2 times
{118, 112, 126} 5 times
{118, 112, 127} 2 times
{120, 112, 127} 4 times
{126, 48, 127} 3 times
{126, 80, 126} 3 times
{126, 80, 127} 2 times

Thus totally repetition occurs for 41 fault location combinations. Hence overall distinguishability factor is

(78 - 41) / 78 *100 = 47.44%.

However, when the individual cases are considered the distinguishability factor can be seen to be appreciably high as seen below:

Same output set of {120, 112, 127} for the following fault combinations

AND-bridging fault at c_3, za_3 lines

AND-bridging fault at za_1, za_3 lines

AND-bridging fault at za_2, zx_1 lines

AND-bridging fault at za_2, zx_2 lines

The distinguishability for this set is(78 - 4) / 78 *100 = 94.87%.

Similarly, the output set {126, 80, 126} occurs 3 times, for which the distinguishability factor is (78 - 3) / 78*100 = 96.15%.

Further, the location of fault can also be easily diagnosed from the output set. For instance if the output set is {120, 112, 127} then the fault condition would be one of the four cases discussed above involving c_3, za_1, za_2, za_3, zx_1, zx_2 and hence those lines only need to be checked.

Similarly, the fault simulations were carried out for the remaining nine random functions and the results are tabulated in Table 4.

TABLE 4

CONSOLIDATED RESULTS FOR AND-BRIDGING FAULTS

S.No.	Function	No. of Data Inputs	Total Possible Faults	Identifiability Factor (%)	Distinguishability Factor (%)
1	F_1	3	78	85.90	47.44
2	F_2	4	136	95.59	36.76
3	F_3	5	231	89.18	47.62
4	F_4	6	351	90.88	52.42
5	F_5	7	210	86.19	48.10
6	F_6	8	820	91.59	58.66
7	F_7	9	465	91.40	47.74
8	F_8	10	496	90.52	33.06
9	F_9	11	465	90.75	38.49
10	F_{10}	12	496	89.11	47.98
	Average			90.11	45.83

4.2 Double Stuck-at Faults

Double Stuck-at faults can occur quite frequently at the adjacent lines of the circuit. The network structure and test vectors are the same as above. However, in the test procedure, two lines at a time are considered and made to be stuck-at-0 or stuck-at-1 and simulated. Since two lines are involved, four possible combinations, viz. (0,0), (0,1), (1,0) and (1,1) with one of the lines as c1 are simulated and tabulated in Tables 5(a),5(b),6(a),6(b),7(a),7(b),8(a) and 8(b).

TABLE 5(a)

DOUBLE STUCK-AT FAULTS OUTPUTS FOR FUNCTION F_1 WITH C_1 AS ONE OF THE LINES FOR 0,0 COMBINATION

	c_1c_2	c_1c_3	c_1c_4	c_1x_1	c_1x_2	c_1x_3
F	126	120	6	120	86	86
O_1	112	112	112	0	0	0
O_2	126	126	126	126	126	126

TABLE 5(b)

	c_1zl_1	c_1za_1	c_1za_2	c_1za_3	c_1zx_1	c_1zx_2
F	46	40	6	46	80	0
O_1	0	112	112	112	112	112
O_2	126	126	126	126	126	126

TABLE 6(a)

DOUBLE STUCK-AT FAULTS OUTPUTS FOR FUNCTION F_1 WITH C_1 AS ONE OF THE LINES FOR 0,1 COMBINATION

	c_1zl_1	c_1za_1	c_1za_2	c_1za_3	c_1zx_1	c_1zx_2
F	118	215	249	209	175	255
O_1	112	112	112	112	112	112
O_2	255	126	126	126	126	126

TABLE 6(b)

	c_1c_2	c_1c_3	c_1c_4	c_1x_1	c_1x_2	c_1x_3
F	126	126	126	126	126	126
O_1	112	112	112	120	116	114
O_2	126	126	126	255	255	255

TABLE 7(a)

DOUBLE STUCK-AT FAULTS OUTPUTS FOR FUNCTION F_1 WITH C_1 AS ONE OF THE LINES FOR 1,0 COMBINATION

	c_1c_2	c_1c_3	c_1c_4	c_1x_1	c_1x_2	c_1x_3
F	38	120	94	32	86	86
O_1	0	0	0	0	0	0
O_2	255	255	255	255	255	255

TABLE 7(b)

	c_1zl_1	c_1za_1	c_1za_2	c_1za_3	c_1zx_1	c_1zx_2
F	46	112	94	46	8	0
O_1	0	0	0	0	0	0
O_2	126	255	255	255	255	255

TABLE 8(a)

DOUBLE STUCK-AT FAULTS OUTPUTS FOR FUNCTION F_1 WITH C_1 AS ONE OF THE LINES FOR 1,1 COMBINATION

	c_1c_2	c_1c_3	c_1c_4	c_1x_1	c_1x_2	c_1x_3
F	38	6	38	38	34	36
O_1	0	0	0	0	0	0
O_2	255	255	255	255	255	255

TABLE 8(b)

	c_1zl_1	c_1za_1	c_1za_2	c_1za_3	c_1zx_1	c_1zx_2
F	118	143	161	209	247	255
O_1	112	0	0	0	0	0
O_2	255	255	255	255	255	255

TABLE 9

CONSOLIDATED RESULTS FOR DOUBLE STUCK-AT FAULTS

S.No.	Function	No. of data Inputs	Total Possible Faults	Identifiability Factor (%)	Distinguishability Factor (%)
1	F_1	3	312	98.40	30.13
2	F_2	4	544	100	31.25
3	F_3	5	924	99.89	33.98
4	F_4	6	1404	99.93	33.26
5	F_5	7	840	100	29.64
6	F_6	8	3280	100	32.50
7	F_7	9	1860	100	32.80
8	F_8	10	1984	100	31.50
9	F_9	11	1860	100	33.12
10	F_{10}	12	1984	100	31.10
	Average			99.82	31.93

From the test results as given in Tables 4, and 9 it was found that the identifiability factor for the set of random functions tested through MATLAB simulation on an average was 90% for AND-bridging faults and almost 100% for Double stuck-at faults , with just n+5 test vectors compared to 2^n test vectors required for conventional testing. It was also observed that the overall distinguishabililty factor was in the range of 30-58%, the individual set distinguishability factor was more than 94% as explained above. The plot for identifiability factor and distinguishability factor for AND-bridging and double stuck-at faults are given in Fig.3 and Fig.4.

Though the overall distinguishability is small, it does not affect the detection capability. Further, the distinguishing capability for an individual output set can be quite high, as illustrated in section 4.1

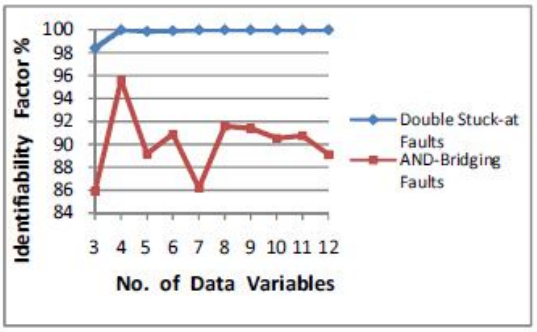

Fig.3 Percentage Identifiability Factor

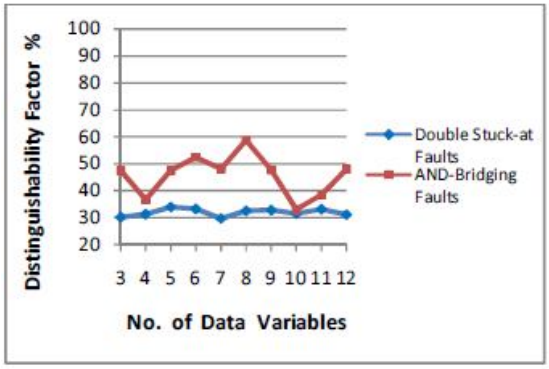

Fig.4 Percentage DistinguishabilityFactor

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5 CONCLUSION

A test set scheme for the detection of AND-bridging and double stuck-at faults for ESOP RMC logic functions have been detailed and the simulation results are shown. The results conclude that n+5 test vectors can be used to detect double stuck-at, and AND-bridging faults in digital circuits. Further, the location can also be diagnosed through the output sets. The analysis and diagnosis have been done through compact tabulation and two quantification indices considering all possible combinations of the data lines, control lines and all intermediate gate outputs line pairs. Detection and distinguishability factors can be further improved by modifying the network structure or using different test vectors.

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